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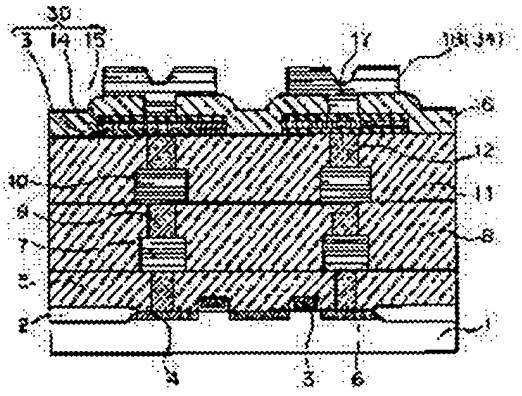
(54) SEMICONDUCTOR DEVICE HAVING CAPACITIVE ELEMENT, AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device using a ceramic thin-film capacitance, in which a multilayer metallic wiring is can be easily formed and deterioration of a capacitive element will not occur.

SOLUTION: The plug of a stack structure of a via 9 and metal wirings 7 and 10 formed simultaneously with the formation of a multilayer metal wiring connects a ceramic thin-film capacitance 30 to a diffusion layer 4. Hydrogen annealing is carried out after the formation of the multilayer metal wiring and prior to the formation of the ceramic thin-film capacitance 30. Since the capacitance 30 is formed after the formation of the multilayer metal wiring, the formation of the multilayer metal wiring



resulting from a capacitance difference will not be prevented. Furthermore, since it is unnecessary to make a via for a tungsten plug after formation of the capacitance, no deterioration of the capacitance takes place by chemical vapor deposition(CVD) method of tungsten. Furthermore, since the capacitance can be formed without modifying a process device in a logical circuit part, existing design parameters can be used.

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* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which has ferroelectric capacity and high dielectric constant object capacity especially, and its manufacture approach about the semiconductor device which has a capacitative element.
[0002]
[Description of the Prior Art] In recent years, research and development in the ferroelectric random-access memory using ferroelectric capacity and the dynamic random access memory (DRAM) using high dielectric constant object capacity etc. is done actively. These ferroelectric random-access memory and DRAMs are equipped with the selection transistor, and are storing information by using as a memory cell capacity connected to one diffusion layer of this selection transistor. Ferroelectric capacity uses ferroelectric thin films, such as Pb(Zr, Ti) O3 (hereafter referred to as "PZT"), as a capacity insulator layer, and can store the information on a non-volatile by carrying out polarization of the ferroelectric. On the other hand, since high dielectric constant object thin films, such as TiO3 (hereafter referred to as "BST"), are used for high dielectric constant object capacity as a capacity insulator layer (Ba, Sr), it can raise the capacitance of capacity and enables detailed-ization of a component.
[0003] In order to operate such a ferroelectric capacity and high dielectric constant object capacity, it is necessary to connect one of the electrodes of capacity to the diffusion layer of a selection transistor electrically as mentioned above.
[0004] Conventionally, in DRAM, the structure which uses as one electrode of capacity polish recon connected to one diffusion layer of a selection transistor, forms SiO2 film, Si3N4 film, etc. in the front face of this polish recon as an insulator layer of capacity, and is made into capacity is common. However, since polish recon will oxidize if it is going to form in the front face of polish recon directly, since it is an oxide, neither a ferroelectric thin film nor a high dielectric constant object thin film (it is henceforth called a "ceramic thin film") can form a good thin film.
[0005] Therefore, 1995 symposium-on, BUIERU S eye digest OBU technical pay parsing (1995 Symposium - VLSI Technology Digest of Technical Papers) In pp.123, the cellular structure which connects a capacity up electrode and a diffusion layer is described by partial wiring of metal which consists of aluminum etc.
[0006] Moreover, International electron Debye Seth meeting technical digest (International electron devices meeting technical digest) The technique which uses TiN barrier metal on polish recon 1994pp.843, and forms PZT capacity is expressed.
[0007] About DRAM, it is an International electron Debye Seth meeting technical digest (Internationalelectron devices meeting technical digest), for example. 1994 SrTiO3 thin film is formed on the RuO2/TiN lower electrode formed on the polish recon plug, and the technique which forms capacity is expressed to pp.841.
[0008] That is, in old ferroelectric random-access memory and formation of DRAM, as mentioned above, after forming capacity, the approach by which metal wiring is formed has been taken.

[0009]
[Problem(s) to be Solved by the Invention] However, there were the following troubles in the memory cell structure of connecting capacity with a diffusion layer with partial wiring or a polish recon plug as mentioned above.
[0010] The 1st trouble is that formation of multilayer metal wiring becomes difficult.
[0011] In order to realize the semiconductor device which integrated highly more the ferroelectric random-access memory and DRAM using a ferroelectric thin film or a high dielectric constant object thin film, and loaded together a logical circuit and such memory, it is necessary to form multilayer metal wiring. On the occasion of formation of multilayer metal wiring, carrying out flattening of the insulator layer between metal wiring layers by the chemical machinery grinding method (the CMP method) etc. is performed.
[0012] However, there is a trouble that originate in formation of capacity, the difference of elevation of the cel array section with capacity and the logical circuit section without capacity becomes large, and the contact after flattening and flattening and connection of the wiring layer by beer become difficult.
[0013] JP,9-92794,A reduces the level difference between a cel and its circumference circuit, and is indicating the manufacture approach of semiconductor memory for the purpose of forming the small multilayer interconnection of the wiring resistance in a circumference circuit.
[0014] In this manufacture approach, the electrode of the capacity of a cel and wiring of those other than a cel field are formed in coincidence. Although noble metals, such as Pt, are usually used for the electrode of capacity using a ceramic thin film, processing is difficult for them, and since these noble metals are high resistance as wiring, it is difficult noble metals to use as wiring of those other than a cel field.
[0015] The 2nd trouble is that the design cost at the time of realizing the semiconductor circuit consolidated with a logical circuit and memory increases.
[0016] The reason is that it becomes impossible that it uses the existing design parameter since it will be necessary to change the process device of a logical circuit for the 1st above-mentioned trouble.
[0017] The 3rd trouble is that the electrical characteristics of capacity deteriorate in the formation process of multilayer metal wiring.
[0018] In multilayer metal wiring, although the tungsten plug is formed, membrane formation of a tungsten (W) is usually performed from the beer which connects between metal wiring in the reaction expressed with a degree type.
[0019]
2WF6+3SiH4 ->2W+3SiH4+6H2, i.e., membrane formation of a tungsten (W), are performed by the very strong reducing atmosphere. Since a ceramic thin film is an oxide, if put to a reducing atmosphere, it will produce an oxygen deficiency. Therefore, there is a trouble of producing the fall (as a result increase of leakage current) of resistance, reduction of a ferroelectric part maximal dose, and degradation of the electrical characteristics of a fall and others of a dielectric constant.
[0020] JP,9-199679,A has proposed the structure of the semiconductor device which avoids reducing atmosphere and makes embedding of a deep contact hole possible. In this semiconductor device, after forming the plug contact which becomes opening which results in the diffusion layer of the store circuit section, and the diffusion layer of the CMOS-circuit section from a heat-resistant metal, capacity besides strong dielectricity is formed and aluminum wiring is further formed to heat-resistant metal plug contact.

[0021] However, in order to realize structure of such a semiconductor device, a complicated production process is needed. Moreover, although the structure of this semiconductor device is applicable to the 1st-layer metal wiring, since membrane formation of a tungsten is required for the beer which connects the 2nd-layer metal wiring and the 1st-layer metal wiring, a solution cannot become to multilayer metal wiring.
[0022] The 4th trouble is that dispersion in the threshold (Vt) of a transistor arises, or a subthreshold level property deteriorates.
[0023] With the interface state density and the fixed charge which were produced in the gate oxide of a

MOS transistor by the plasma damage in plasma etching etc., dispersion arises in the threshold (Vt) of a transistor, or a subthreshold level property deteriorates.

[0024] As the technique of improving these, annealing (hydrogen annealing) in the inside of the ambient atmosphere containing hydrogen is performed from the former. However, about the semiconductor device which has a capacitative element using a ceramic thin film, if such annealing is performed after forming a capacitative element as the 3rd trouble described, since degradation of the electrical characteristics of capacity will be produced, such annealing cannot perform after formation of a capacitative element.

[0025] The technique of preparing the hydrogen barrier film of Si3N4 grade on capacity is indicated by JP,7-111318,A there. By preparing the hydrogen barrier film on capacity, this technique prevents and has diffusion of the hydrogen to capacity, and prevents degradation of the capacitative element in a reducing atmosphere.

[0026] However, it set on this technique, and since the process in which the hydrogen barrier film is formed and processed increases, the new problem of ****, as a result the manufacture increase in cost of a routing counter has been brought about.

[0027] And when applying this technique to the component made high integration and detailed more, the hydrogen barrier film is also asked for thin film-ization. However, if the hydrogen barrier film is thin-film-ized, the problem that hydrogen barrier property becomes inadequate will be caused.

[0028] In connection with large-scale-izing and improvement in the speed of a semiconductor device in recent years, and detailed-izing of a component on the other hand, reduction of dispersion in transistor characteristics is more important still.

[0029] After the 5th trouble forms capacity, when the contact which connects metal wiring and metal wiring, and a substrate is formed like before, it is causing the increment in the wiring resistance which connects degradation of capacitance characteristics, and capacity and other components.

[0030] Usually, the ion implantation is performed, after puncturing contact in order to reduce resistance between metal wiring and a substrate in case the contact which connects metal wiring and a substrate is formed. Therefore, it needs to perform heat treatment at the temperature beyond about 700 degrees C or it after an ion implantation for ion activation.

[0031] However, if such hot heat treatment is performed after forming ceramic thin film capacity, a ceramic, an electrode, and wiring will cause a mutual reaction and counter diffusion. For this reason, degradation of capacitance characteristics and the increment in wiring resistance take place as mentioned above.

[0032] As an approach of solving degradation of the capacitative element by elevated-temperature heat treatment after such capacitative element formation, the manufacture approach of the semiconductor memory which forms capacity after forming metal wiring is stated to JP,6-85187,A. According to this manufacture approach, the capacitative element and the substrate are connected by carrying out opening of the contact which connects the diffusion layer of a substrate with the are recording electrode of capacity, and forming a capacity are recording electrode after that after metal wiring formation.

[0033] However, with such structure, when metal wiring is two-layer or more than it, a contact hole becomes remarkably deep and forming the are recording electrode of capacity into it is accompanied by the problem of being remarkably very difficult.

[0034] Neither the ferroelectric random-access memory using multilayer metal wiring structure nor ceramic thin film capacity DRAM is yet realized by the above troubles.

[0035] It aims at offering the semiconductor device using the ceramic thin film capacity which this invention is made in view of the trouble in the semiconductor device which has the above conventional capacitative elements, and can form multilayer metal wiring easily, and does not produce degradation of a capacitative element.

[0036] Moreover, this invention aims at offering the semiconductor device which can realize the chip which loaded together a logical circuit and the memory which used ceramic thin film capacity by low cost.

[0037] Furthermore, this invention aims at offering the semiconductor device which has good transistor

characteristics, using ceramic thin film capacity.
[0038]
[Means for Solving the Problem] The semiconductor device by this invention is characterized by considering as the memory cell structure of connecting capacity and a diffusion layer, by the plug which consists of structure which carried out the laminating of the metal wiring to the beer formed in formation and coincidence of multilayer metal wiring to the memory cell structure of connecting capacity with a diffusion layer with partial wiring or a polish recon plug like before.
[0039] Therefore, formation of multilayer metal wiring is not barred for the difference of elevation by capacity. Moreover, since capacity can be formed without changing the process device of the logical circuit section in any way, the existing design parameter can be used as it is.
[0040] Specifically, claim 1 offers the semiconductor device with which the lower electrode with which a substrate, metal wiring of at least one layer, a lower electrode and a ceramic thin film, and an up electrode constitute ceramic thin film capacity in the semiconductor device which has the ceramic thin film capacity which comes to carry out a laminating to this order, a ceramic thin film, and an up electrode are characterized by being formed above metal wiring of at least one layer among this inventions.
[0041] One [at least] electrode is connected with the substrate through wiring among the electrodes which constitute ceramic thin film capacity, and it is desirable to constitute so that the wiring may include metal wiring of at least one layer as indicated by claim 2.
[0042] When connecting ceramic thin film capacity and a substrate through wiring, as indicated by claim 3 moreover, this wiring The structure which carried out the laminating of the beer which connects the contact, metal wiring, this metal wiring, and one electrode of ceramic thin film capacity which connect metal wiring and a substrate, Or it is desirable to constitute so that it may have the structure where the laminating of at least one metal wiring and the beer was carried out between metal wiring and one electrode of ceramic thin film capacity.
[0043] Or when connecting one [at least] electrode of ceramic thin film capacity to a substrate through wiring as indicated by claim 4, at least, this wiring is the contact formed after much more metal wiring and this metal wiring, and it is desirable to consider as structure including the contact which connects either and the substrate of one or metal wiring of the electrode of ceramic thin film capacity.
[0044] Or when connecting one [at least] electrode of ceramic thin film capacity to a substrate through wiring as indicated by claim 5, as for this wiring, it is desirable to have the structure which carried out the direct laminating of at least one contact or the beer.
[0045] Such concrete structures shown in claim 1 thru/or 5 can attain above-mentioned effectiveness.
[0046] It is also possible to form much more metal wiring in the upper part of ceramic thin film capacity further at least as indicated by claim 6.
[0047] Further multilayer metal wiring can be formed by this. Especially, generally in multilayer metal wiring in large-scale LSI in recent years, wiring width of face and the tooth space between wiring are large by the upper wiring as compared with lower layer wiring. For this reason, even if it forms ceramic thin film capacity between metal wiring layers, the level difference produced by it does not have a bad influence on the upper metal wiring formation.
[0048] Moreover, as for metal wiring formed in the upper part of ceramic thin film capacity, it is desirable like claim 7 to be used only as a plate line of the memory equipped with the memory cell which contains ceramic thin film capacity at least.
[0049] Moreover, it is desirable to form as the beer or contact which connects one of the electrodes of ceramic thin film capacity with metal wiring or a substrate is carrying out eccentricity from the center of ceramic thin film capacity as indicated by claim 8. That is, it is desirable that beer or contact is not formed in the center of ceramic thin film capacity.
[0050] The area of capacity can be made to increase by such configuration, without making cel area increase.
[0051] Moreover, as for the contact currently formed in the lower part of ceramic thin film capacity, arranging so that eccentricity may be carried out is desirable [the contact currently formed in the upper

part of ceramic thin film capacity] as indicated by claim 9.
[0052] By this configuration, the margin between contacts and capacity of the capacity upper part can be enlarged.
[0053] Ceramic thin film capacity can be formed in various gestalten.
[0054] For example, the up electrode which forms ceramic thin film capacity has an area smaller than a lower electrode, and it can form it as the laminating is carried out, as indicated by claim 10.
[0055] By considering as such a configuration, it can prevent that an up electrode and a lower electrode short-circuit in a capacity side attachment wall.
[0056] or the whole surface of the both sides of two or more lower electrodes which ceramic thin film capacity opened spacing on the interlayer insulation film, and were formed as indicated by claim 11, and an interlayer insulation film and a lower electrode -- a wrap ceramic thin film and some lower electrodes [at least] -- a wrap -- the up electrode currently formed on the ceramic thin film like -- since -- constituting is also possible.
[0057] According to this gestalt, since it is not necessary to process a ceramic thin film into predetermined magnitude, only that part can simplify a manufacture process.
[0058] Between ceramic thin film capacity and the interlayer insulation film of the lower part, the diffusion barrier film can also be formed as indicated by claim 12.
[0059] Since there is a possibility that the element which constitutes a ceramic thin film may be spread in an interlayer insulation film in forming a ceramic thin film after processing a lower electrode especially, this diffusion can be prevented by forming the diffusion barrier film.
[0060] As for the contact which connects the lower electrode of ceramic thin film capacity, and metal wiring located under this ceramic thin film capacity, and the beer currently formed under this metal wiring, it is desirable to open and arrange spacing through this metal wiring as indicated by claim 13.
[0061] Depending on the formation process of beer and metal wiring, a crater may be produced in metal wiring on beer. Thus, if contact and beer are formed on metal wiring which is not flat, good electrical installation may not be obtained. For this reason, the defect of electrical installation can be prevented by forming contact in the location detached to some extent instead of right above of beer.
[0062] When metal wiring of a bilayer is formed at least between ceramic thin film capacity and a substrate, upper metal wiring can also carry out direct continuation to a substrate through contact as indicated by claim 14.
[0063] Since downward metal wiring can be used only as bit wiring for example, in a cel according to this configuration, cel area can be made to reduce.
[0064] It is also possible to form plate line backing wiring above ceramic thin film capacity as indicated by claim 15.
[0065] According to this configuration, wiring resistance of a plate line can be decreased.
[0066] Moreover, backing wiring of a word line can also form with downward metal wiring rather than ceramic capacity as indicated by claim 16.
[0067] In this case, it is desirable that backing wiring of an adjacent word line is formed with two-layer metal wiring at least as indicated by claim 17.
[0068] Furthermore, since crossing at least in a memory cell array in the piece place can reduce a noise, two-layer metal wiring which forms word line backing wiring has it, as indicated by claim 18.
[desirable]
[0069] When forming metal wiring above ceramic thin film capacity through an interlayer insulation film as indicated by claim 19, this metal wiring can be connected to metal wiring or the substrate formed under the ceramic thin film capacity in the end through the crevice formed over the both sides of the interlayer insulation film formed under an interlayer insulation film and the ceramic thin film capacity.
[0070] Or it connects with the beer formed under the ceramic thin film capacity through the crevice formed in the interlayer insulation film, and you may make it connect metal wiring to metal wiring or the substrate formed under the ceramic thin film capacity through this beer in the end as indicated by claim 20.
[0071] As indicated by claim 21 or metal wiring In the end, the crevice formed over the both sides of an

interlayer insulation film and the ceramic thin film of ceramic thin film capacity is minded. It connects with the lower electrode of ceramic thin film capacity, and connects with the beer formed under the ceramic thin film capacity through this lower electrode, and you may make it make it connect with metal wiring or the substrate formed under the ceramic thin film capacity through this beer.
[0072] According to which [these / three] gestalt, if connection between the above-mentioned metal wiring and a diffusion layer is made, after formation of ceramic thin film capacity, it becomes unnecessary to use CVD of a tungsten and degradation of ceramic thin film capacity can be prevented.
[0073] When using an up electrode as a plate line, this up electrode can be connected to metal wiring or the substrate formed under the ceramic thin film capacity in the end through the crevice formed over the both sides of the interlayer insulation film formed under the ceramic thin film of ceramic thin film capacity, and this ceramic thin film capacity as indicated by claim 22.
[0074] As indicated by claim 23 or an up electrode In the end, the crevice formed in the ceramic thin film of ceramic thin film capacity is minded. It connects with the lower electrode of ceramic thin film capacity, and connects with the beer formed under the ceramic thin film capacity through this lower electrode, and you may make it make it connect with metal wiring or the substrate formed under the ceramic thin film capacity through this beer.
[0075] Metal wiring can use aluminum or copper as a principal component as indicated by claim 24.
[0076] Moreover, the beer or contact which connects one of the electrodes of ceramic thin film capacity with metal wiring or a substrate can use a tungsten as a principal component as indicated by claim 25.
[0077] The lower electrode of ceramic thin film capacity shall contain a conductive nitride as indicated by claim 26.
[0078] Moreover, as for a conductive nitride, it is desirable that they are titanium nitride, tantalum nitride, or a nitriding tungsten as indicated by claim 27.
[0079] Furthermore, a lower electrode can be considered as the configuration which carried out the laminating of the layer containing a conductive nitride, and the noble-metals layer as indicated by claim 28.
[0080] In this case, as for a noble-metals layer, it is desirable to carry out the laminating of platinum, iridium, rutheniums, these alloys, or these as indicated by claim 29.
[0081] the first process which forms metal wiring with claim 30 much more at least, and the second process which forms ceramic thin film capacity after this first process -- since -- the manufacture approach of the becoming semiconductor device is offered.
[0082] By the approach concerning this claim 30, the semiconductor device concerning above-mentioned claim 1 can be formed.
[0083] Furthermore, after forming multilayer metal wiring, in order to form ceramic thin film capacity according to this approach, it is not necessary to form the beer by the tungsten plug after ceramic thin film capacity formation. Therefore, ceramic thin film capacity does not deteriorate by CVD of a tungsten.
[0084] Moreover, since contact to metal wiring and a substrate is also formed before formation of ceramic thin film capacity, degradation of ceramic thin film capacity and the increment in wiring resistance resulting from the activation after contact impregnation can be prevented.
[0085] Moreover, as for an above-mentioned approach, it is desirable to have the process in which annealing is performed in the ambient atmosphere containing hydrogen as indicated by claim 31.
[0086] A deterioration of the transistor can be reduced by this hydrogen annealing.
[0087] As for the temperature of this hydrogen annealing, it is desirable that it is [300 degree Centigrade to 500 degree Centigrade] the range as indicated by claim 32.
[0088] The effectiveness of an improvement of transistor characteristics is small less than at 300-degree Centigrade, and it is because there is a possibility of causing an open circuit of metal wiring more than in 500-degree Centigrade.
[0089] moreover, the second process in which claim 33 forms at least metal wiring as some wiring which connects the first process which forms much more metal wiring, and one [at least] electrode and substrate of ceramic thin film capacity -- since -- the manufacture approach of the becoming

semiconductor device is offered.
[0090] The semiconductor device concerning claim 2 can be manufactured by this approach.
[0091] Ceramic thin film capacity can be formed by various approaches.
[0092] for example, the first process which forms a lower electrode as ceramic thin film capacity is indicated by claim 34, the second process which forms a ceramic thin film on a lower electrode, the third process which forms an up electrode on a ceramic thin film, and the fourth process which etches a lower electrode, a ceramic thin film, and an up electrode -- since -- it can form.
[0093] or the first process which forms a lower electrode as indicated by claim 35, and etches this, the second process which forms a ceramic thin film on a lower electrode, and the third process which forms an up electrode on a ceramic thin film, and etches this -- since -- it can also form.
[0094] As for a ceramic thin film, it is desirable to be formed at the temperature of 500-degree less than Centigrade as indicated by claim 36 in these cases.
[0095] Although the membrane formation more than in 600-degree Centigrade is required of a usual sol-gel method and the usual sputtering method in order to obtain a good ceramic thin film, at such an elevated temperature, an open circuit of metal wiring and high resistance-ization are caused. For this reason, membranes can be formed at the low temperature of 500-degree less than Centigrade by using a CVD method.
[0096] When forming a ceramic thin film like the approach indicated to claim 35 after processing a lower electrode, as indicated to claim 37, it is desirable to have further the process which forms the diffusion barrier film between a lower electrode and the interlayer insulation film of the lower part of this lower electrode.
[0097] Much more metal wiring may be further formed in the upper part of ceramic thin film capacity at least as indicated by claim 38.
[0098] A thereby further multilayer metal wiring layer can be formed.
[0099] In this case, as for metal wiring formed in the upper part of ceramic thin film capacity, it is desirable to be formed in the ambient atmosphere where reducibility is weak as indicated by claim 39.
[0100] Thereby, degradation of the ceramic thin film capacity located under the metal wiring can be prevented.
[0101] The process in which claim 40 forms an interlayer insulation film on ceramic thin film capacity, It is the manufacture approach of the semiconductor device further equipped with the process which forms the first metal wiring connected to ceramic thin film capacity through an interlayer insulation film. The first metal wiring In the end, it passes into the possession of the both sides of the interlayer insulation film formed under an interlayer insulation film and the ceramic thin film capacity, and after forming the crevice which results in the second metal wiring formed under the ceramic thin film capacity, the approach of being what is formed in a crevice is offered.
[0102] The semiconductor device concerning claim 19 can be offered by this approach.
[0103] The process in which claim 41 forms an interlayer insulation film on ceramic thin film capacity, It is the manufacture approach of the semiconductor device further equipped with the process which forms the first metal wiring connected to ceramic thin film capacity through an interlayer insulation film. The first metal wiring In the end, after forming a crevice in an interlayer insulation film, it is formed in this crevice and metal wiring of this first offers the approach of being what is connected with the second metal wiring formed under the ceramic thin film.
[0104] By this approach, the semiconductor device concerning claim 20 or claim 21 can be offered.
[0105] Claim 42 crosses the up electrode of ceramic thin film capacity to the both sides of the interlayer insulation film formed under the ceramic film and this ceramic thin film capacity in the end, and after forming the crevice which results in the second metal wiring formed under the ceramic thin film capacity, the manufacture approach of the semiconductor device characterized by being what formed in said crevice is offered.
[0106] The semiconductor device concerning claim 22 can be offered by this approach.
[0107] Claim 43 is formed in this crevice, after the up electrode of ceramic thin film capacity forms a crevice in the ceramic film in the end, and this up electrode offers the approach of being what is

connected with the second metal wiring formed under the ceramic thin film capacity through the beer formed under the lower electrode of ceramic thin film capacity, and this lower electrode.
[0108] The semiconductor device concerning claim 23 can be offered by this approach.
[0109]
[Embodiment of the Invention] (First operation gestalt) Some top views of the ferroelectric random-access memory as first operation gestalt concerning this invention or the memory cell of DRAM are shown in drawing 1 . Drawing 1 (A) is a top view when seeing a memory cell from the upper part, until after forming the first metal wiring, and drawing 1 (B) is a top view when seeing the memory cell after forming the first metal wiring from the upper part. Drawing 2 is the sectional view which met the A-A line of drawing 1 (A). Moreover, drawing 3 is the circuit diagram of the memory cell shown in drawing 1 .
[0110] As shown in drawing 3 , the memory cell 32 is equipped with the selection transistor 31 and the ceramic thin film capacity 30. Another side is connected [the gate of the selection transistor 31] to the bit line 35 on the plate line 34 through the ceramic thin film capacity 30 at the word line 33, respectively for either the source or a drain.
[0111] As shown in drawing 2 , on the silicon substrate 1, the MOS transistor as a selection transistor 31 shown in drawing 3 is formed. On this MOS transistor, the 1st metal wiring 7 which consists of an alloy which uses barrier metal, such as Ti, and aluminum or Cu as a principal component is formed, and it connects with each diffusion layer 4 of a MOS transistor through the contact 6 which consists of a tungsten plug etc.
[0112] Among two 1st metal wiring 7 shown in drawing 1 , one 1st metal wiring 7 is used as wiring which connects the ceramic thin film capacity 30 and the selection transistor 31, and the 1st metal wiring 7 of another side is used as a bit line 35. After the 1st metal wiring 7, the 2nd metal wiring 10 which consists of an alloy which uses barrier metal, such as Ti, and aluminum or Cu as a principal component like the 1st metal wiring 7 is formed, and the 2nd metal wiring 10 is electrically connected with the 1st metal wiring 7 through the beer 9 which consists of a tungsten plug etc. like contact 6. Thus, in the memory cell 32 concerning this operation gestalt, the multilayer metal wiring structure which consists of the 1st metal wiring 7 and the 2nd metal wiring 10 is formed.
[0113] The ceramic thin film capacity 30 is formed on this multilayer metal wiring structure. The laminating of the lower electrode 13, the ceramic thin film 14, and the up electrode 15 is carried out to this order, and the ceramic thin film capacity 30 is constituted.
[0114] The lower electrode 13 of the ceramic thin film capacity 30 is connected with the 2nd metal wiring 10 through the capacity lower contact 12. Consequently, it means that connection between the ceramic thin film capacity 30 and the selection transistors 31 in drawing 3 was made.
[0115] On the ceramic thin film capacity 30, the 3rd metal wiring 18 is formed through the capacity up contact 17. The 3rd metal wiring 18 is used as a plate line 34 in drawing 3 .
[0116] Thus, downward structure is completely the same as that of LSI without the usual ceramic thin film capacitative element than the 2nd metal wiring 10 of the memory cell 32 in this operation gestalt. Therefore, it can manufacture in the same manufacture process as LSI.
[0117] Therefore, according to this operation gestalt, the effectiveness that the semiconductor device which loaded together the ferroelectric random-access memory or DRAM using such a memory cell 32, and the usual logic LSI on the 1 chip is realizable by low cost using the existing logical circuit is brought about.
[0118] In addition, the properties searched for with the cel transistor 31 of the memory cell used for ferroelectric random-access memory or DRAM and the transistor of the usual logical circuit differ. Therefore, the cel transistor 31 may be made into different structure from the transistor of a logical circuit. For example, since impressing an electrical potential difference higher than the operating voltage of a memory circuit is generally performed, a word line 33 may need to make gate thickness thicker than the transistor of other logical circuits. Thus, generally forming the transistor from which structure differed on the same substrate is performed as stated to the 55-page Nikkei micro device March, 1995 issue, and it is realizable using the manufacture process of the usual logical circuit.

[0119] How to manufacture the semiconductor device equipped with the memory cell 32 concerning this operation gestalt is shown in drawing 4 thru/or drawing 6 .
[0120] First, as shown in drawing 4 (A), MOS transistors, such as the memory cell section and the logical-circuit section, are formed on a silicon substrate 1 according to the manufacture process of the usual LSI. That is, an oxide film 2 is formed on a silicon substrate 1, with an oxide film 2, a component formation field is demarcated and, subsequently the gate electrode 3 and a diffusion layer 4 are formed. Furthermore, the 1st interlayer insulation film 5 is formed on a silicon substrate 1. Flattening of the 1st interlayer insulation film 5 which formed membranes is carried out by the CMP method, the reflow method, etc.
[0121] Next, the contact 6 which connects the 1st metal wiring 7, the 1st metal wiring 7, and a diffusion layer 4 is formed.
[0122] There are an approach of forming and processing the 1st metal wiring 7 as these formation approaches after forming contact 6 by a tungsten plug etc., and the dual DAMASHIN method which embeds metal, removes an excessive metal after that, and forms contact 6 and the 1st metal wiring 7 in coincidence after processing an interlayer insulation film 5 into the configuration of contact 6 and the 1st metal wiring 7.
[0123] After puncturing contact 6 by etching in the case of the former, contact impregnation and activation are performed and barrier metal, such as Ti and TiN, is formed. Then, a tungsten is formed all over a wafer with a CVD method, subsequently, the CMP method and etchback remove a surface tungsten and a tungsten plug is formed. A tungsten plug can also be formed with the selective growth of a tungsten.
[0124] Subsequently, as shown in drawing 4 (B), the 1st metal wiring 7 is formed after contact 6. After the 1st metal wiring 7 being constituted by the compound layer which consists of antireflection films which use barrier metal, such as Ti and TiN, aluminum, Cu, etc. as a principal component, such as an alloy layer and TiN, and depositing it with the sputtering method or a CVD method, respectively, it is processed by etching.
[0125] Then, as shown in drawing 5 (C), after forming and carrying out flattening of the 2nd interlayer insulation film 8, beer 9 and the 2nd metal wiring 10 are formed on the 1st metal wiring 7. Beer 9 and the 2nd metal wiring 10 are formed by the same approach as contact 6 and the 1st metal wiring 7.
[0126] Then, as shown in drawing 5 (D), after forming the 3rd interlayer insulation film 11, the capacity lower contact 12 is formed by a tungsten plug etc. like contact 6 on the 2nd metal wiring 10. Under the present circumstances, it is desirable to perform removal of a surface tungsten by the CMP method. It is because the ceramic thin film capacity 30 formed behind can be formed on a completely flat front face.
[0127] Then, annealing is performed in the ambient atmosphere containing hydrogen. 300 degrees C or more 500 degrees C or less of annealing temperature are desirable. Below 300 degrees C, the effectiveness of a transistor-characteristics improvement is small and it is because there is a possibility of causing an open circuit of the metal wiring 7 and 10 etc., above 500 degrees C.
[0128] The above process is the same as the usual LSI process of not having ceramic thin film capacity. Modification or the addition of a special process for connecting ceramic thin film capacity to a diffusion layer 4 are not performed at all.
[0129] Subsequently, the ceramic thin film capacity 30 is formed so that it may connect with the capacity lower contact 12 on the 3rd interlayer insulation film 11. The ceramic thin film capacity 30 is formed in the following procedures.
[0130] First, as shown in drawing 6 (E), noble metals, such as Pt, Ir, and Ru, or IrO2, and the lower electrode 13 that consists of a conductive oxide of RuO2 grade are formed on the 3rd interlayer insulation film 11 by the approach of the sputtering method and others.
[0131] In this case, in order to prevent a mutual reaction and counter diffusion, such as a tungsten of the capacity lower contact 12, and Pt of the lower electrode 13, it is desirable to form in the bottom of these noble metals or a conductive oxide layer the barrier film which consists of TiN etc.
[0132] Subsequently, the ceramic thin film 14 which consists of Pb(Zr, Ti) O3 (PZT), TiO (Ba, Sr)3 (BST), SrTiO3 (ST), etc. is formed with a CVD method etc. on the lower electrode 13.

[0133] When forming PZT, by a usual sol-gel method and the usual sputtering method, heating at 600 degrees C or more is required to obtain a good PZT thin film. At such an elevated temperature, an open circuit of metal wiring and high resistance-ization are caused, and it cannot apply to this structure. Therefore, it is desirable like a CVD method to form membranes at about 500-degree C low temperature.
[0134] In a 350 to 500 degrees C temperature requirement, a PZT thin film can form the good film with a CVD method. moreover, ST film -- for example, international Electron Debye Seth a meeting -- technical Digest (International electron devices meeting technical digest) 1994 It can form at 450 degrees C with an ECR-CVD method as stated to pp.831.
[0135] On the ceramic thin film 14 formed by the above approaches, the up electrode 15 is formed by the same approach as the lower electrode 13.
[0136] Then, the up electrode 15, the ceramic thin film 14, and the lower electrode 13 are processed by etching. Thus, the ceramic thin film capacity 30 as shown in drawing 6 (E) is formed.
[0137] Furthermore, after forming the 4th interlayer insulation film 16 on the ceramic thin film capacity 30, the capacity up contact 17 is punctured. Then, as shown in drawing 6 (F), the 3rd metal wiring 18 used as the plate line 34 is formed like the 1st and 2nd metal wiring 7 and 10.
[0138] The 3rd metal wiring 18 is used only as a plate line 34, and is not used in other logical-circuit sections. Therefore, in the logical-circuit section, there is no modification of the device by forming the memory cell array section using the ceramic thin film capacity 30. The passivation film (not shown) which consists of SiON etc. is formed after this 3rd metal wiring 18.
[0139] The plate line 34 is usually connected to the inverter of a plate line drive circuit in the end of a cel array. How to connect to a diffusion layer 4 hereafter the 3rd metal wiring 18 used as a plate line 34 is explained using drawing 7 and drawing 8 .
[0140] Drawing 7 is the sectional view having shown an example of structure which connects the 3rd metal wiring 18 (plate line 34) to a diffusion layer 4.
[0141] As shown in drawing 7 , the plate line contact 19 penetrated the 4th interlayer insulation film 16, and even the 2nd metal wiring 10 has attained it in the 3rd interlayer insulation film 11. In the plate line contact 19, it connects with the 2nd metal wiring 10 directly, and the 3rd metal wiring 18 is connected to the diffusion layer 4 through beer 9, the 1st metal wiring 7, and contact 6. Such structure can be manufactured as follows.
[0142] First, after forming the 4th interlayer insulation film 16 on the ceramic thin film capacity 30, the plate line contact 19 and the capacity up contact 17 are punctured. Then, the 3rd metal wiring 18 is formed. Thus, the contact to the up electrode 15 and contact to the 2nd metal wiring 10 can be formed in coincidence.
[0143] Drawing 8 is the sectional view having shown other examples of the structure of connecting the 3rd metal wiring 18 (plate line 34) to a diffusion layer 4.
[0144] As shown in drawing 8 , the plate line contact 19 which arrives at the front face of the 3rd interlayer insulation film 11 is formed in the 4th interlayer insulation film 16. Through the 2nd beer 20, it connects with the 2nd metal wiring 10, as a result the 3rd metal wiring 18 is connected to the diffusion layer 4 through beer 9, the 1st metal wiring 7, and contact 6. Such structure can be manufactured as follows.
[0145] When forming the capacity lower contact 12, the 2nd beer 20 is formed in coincidence. Then, after forming the ceramic thin film capacity 30 and the 4th interlayer insulation film 16, the plate line contact 19 is punctured. Then, the 3rd metal wiring 18 is formed. Thus, the contact to the up electrode 15 and contact to the 2nd metal wiring 10 can be formed in coincidence.
[0146] If connection between the 3rd metal wiring 18 and a diffusion layer 4 is formed by the approach [like / above-mentioned / two], after forming the ceramic thin film capacity 30, it is not necessary to use CVD of a tungsten, and degradation of the ceramic thin film capacity 30 will not arise.
[0147] In this operation gestalt, since the process in which the ceramic thin film capacity 30 is formed is adopted after forming multilayer metal wiring, formation of multilayer metal wiring is not barred for the difference of elevation resulting from the ceramic thin film capacity 30.

[0148] Moreover, it is not necessary to form contact to tungsten plug structure, or metal wiring and a substrate after formation of the ceramic thin film capacity 30. Therefore, tungsten - A ceramic thin film capacitative element does not deteriorate by CVD and heat-of-activation processing.
[0149] Furthermore, it is, after forming a multilayer interconnection, and since hydrogen annealing is performed before formation of the ceramic thin film capacity 30, while being able to reduce dispersion in the threshold Vt of a transistor, degradation of a ceramic thin film capacitative element is not caused.
[0150] Moreover, in this operation gestalt, plug wiring which connects the ceramic thin film capacity 30 and the selection transistor 31 to formation and coincidence of multilayer metal wiring is formed. Therefore, it is not necessary to prepare independently the plug for connecting the ceramic thin film capacity 30 and the selection transistor 31, and the advantage that a manufacture process can be simplified is also acquired.
[0151] The first above-mentioned operation gestalt can apply this invention also about the case where further multilayer metal wiring is used, although it is the example which applied this invention when ceramic thin film capacity was formed on two-layer metal wiring. Even in such a case, by the completely same approach as this operation gestalt, after forming multilayer metal wiring, ceramic thin film capacity can be formed.
[0152] With the first above-mentioned operation gestalt, although the 3rd metal wiring 18 is metal wiring of the maximum upper layer, it can also form multilayer metal wiring further on this.
[0153] In large-scale LSI in recent years, the structure of multilayer metal wiring of forming partial wiring to which between the components which approached is connected with lower layer metal wiring, and forming the so-called far-reaching global wiring, such as a power-source line, with the upper metal wiring is adopted. In such a case, in the upper metal wiring, it is common that wiring width of face and the tooth space during wiring are large compared with lower layer metal wiring. For this reason, even if it forms ceramic thin film capacity between metal wiring of a vertical layer, the level difference produced by it does not have a bad influence on formation of the upper metal wiring.
[0154] Furthermore, if the upper metal wiring is formed by the approach used as strong reducing atmospheres, such as sputtering and plating, degradation of ceramic thin film capacity will not be caused.
[0155] Next, the concrete example at the time of applying this operation gestalt to ferroelectric random-access memory is explained using drawing 4 thru/or drawing 6 .
[0156] First, the oxide film 2 was formed on the silicon substrate 1 by wet oxidation. Then, the ion implantation of the impurities, such as boron and Lynn, was carried out to the silicon substrate 1, and the well of n mold and p mold was formed. Then, the gate 3 and a diffusion layer 4 were formed as follows.
[0157] First, after forming gate oxide by wet oxidation, the polish recon used as the gate 3 was formed and etched. On this polish recon film, after forming silicon oxide, it etched and the side-attachment-wall oxide film was formed.
[0158] Next, the ion implantation of the impurities, such as boron and arsenic, was carried out, and the diffusion layer 4 of n mold and p mold was formed.
[0159] Furthermore, after forming Ti film on this, Ti silicide was formed in the gate 3 and a diffusion layer 4 by making it react with silicon and removing unreacted Ti by etching.
[0160] According to the above process, as shown in drawing 4 (A), the MOS transistor of n mold and p mold was formed in the silicon substrate 1.
[0161] Next, the 1st metal wiring layer 7 and the 2nd metal wiring layer 10 were formed as follows.
[0162] First, after forming the silicon oxide (BPSG) which contained impurities, such as silicon oxide and boron, as the 1st interlayer insulation film 5 on a silicon substrate 1, flattening was carried out by the CMP method.
[0163] Next, after puncturing contact 6 by etching, the impurity was poured in to the diffusion layer 4 of n mold and each p mold, and heat treatment for 10 seconds was performed at 750 degrees C. Then, Ti and TiN were formed as a barrier metal. After forming a tungsten with a CVD method besides, the surface tungsten was removed by the CMP method. Then, as the 1st metal wiring 7, AlCu was formed by sputtering and it was processed by etching.

[0164] After forming silicon oxide with a CVD method as the 2nd interlayer insulation film 8 after this 1st metal wiring 7, flattening was carried out by the CMP method. Beer 9 was formed by the same approach as contact 6, and by the same approach as the 1st metal wiring, as shown in drawing 5 (C), it formed the 2nd metal wiring 10.
[0165] Furthermore, as shown in drawing 5 (D), the capacity lower contact 12 was formed by the same approach as contact 6 after forming the 3rd interlayer insulation film 11. Then, annealing for 20 minutes was performed at the temperature of 400 degrees C under the ambient atmosphere of 5% of hydrogen, and 95% of nitrogen.
[0166] Next, the formation approach of the ferroelectric capacity 30 is explained.
[0167] First, TiN of 50nm of thickness and Pt of 100nm of thickness were formed by the sputtering method in this order as a lower electrode 13. When sputtering is performed at the temperature of 300 degrees C or more, since crystallinity of Pt improves, it is desirable.
[0168] Then, PZT was formed with the CVD method as a ferroelectric thin film 14 on the lower electrode 13.
[0169] NO2 was used for the raw material as an oxidizer using bis-dipivaloyl meta-NATO lead (Pb2 (DPM)) and titanium iso polo POKISHIDO (Ti4 (OiPr)) and zirconium butoxide (Zr4 (OtBu)).
[0170] These organic metal raw materials and oxidizers were supplied in the reaction chamber from the separate feed hopper. Membrane formation conditions made substrate temperature 400 degrees C, and total pressure of the gas of the membrane formation interior of a room was set to 5x10-3Torr. First, flow rate 0.2SCCM and Ti (OiPr)4 were formed by flow rate 0.25SCCM, and NO2 was formed for Pb(DPM) 2 for 40 seconds on condition that flow rate 3.0SCCM. By this, the very small nuclear crystal of PbTiO3 was formed on the lower electrode 13.
[0171] Then, flow rate 0.225SCCM and Ti (OiPr)4 were formed by flow rate 0.2SCCM, NO2 was formed [Pb (DPM)2] for flow rate 0.25SCCM and Zr (OtBu)4 for 600 seconds on condition that flow rate 3.0SCCM, and the PZT film 14 of 100nm of thickness was obtained.
[0172] Then, annealing for 10 minutes was performed at the temperature of 400 degrees C under the ambient atmosphere of 100% of oxygen. Before forming the up electrode 15, the electrical characteristics of PZT capacity can be raised by performing annealing.
[0173] IrO2 of 50nm of thickness and Ir of 100nm of thickness were formed by the sputtering method as an up electrode 15 on the PZT film 14 at this order.
[0174] Then, the up electrode 15, the PZT film 14, and the lower electrode 13 were processed by etching, and further, annealing for 10 minutes was performed at the temperature of 400 degrees C under the ambient atmosphere of 100% of oxygen, and it considered as the PZT capacity 30.
[0175] If annealing is further performed after forming the up electrode 15, the impression direction dependency of the electric field of the PZT capacity 30 becomes small, and a symmetrical hysteresis characteristic can be acquired.
[0176] After forming silicon oxide by O3 TEOS-CVD as the 4th interlayer insulation film 16, the capacity up contact 17 and the plate line contact 19 were punctured by etching.
[0177] Subsequently, in order to recover degradation of the PZT capacity 30 by etching, annealing was performed for 10 minutes at the temperature of 400 degrees C under nitrogen-gas-atmosphere mind.
[0178] After forming WSi, TiN, AlCu, and TiN by sputtering in this order as the 3rd metal wiring 18, it was processed by etching.
[0179] After forming silicon oxide and the SiON film by plasma CVD as passivation film (not shown) besides, the polyimide film was formed further. Then, the wiring pad section was punctured and electrical characteristics were evaluated. The result is shown below.
[0180] When the PZT capacity of 1-micrometer angle was connected to 5000-piece juxtaposition and the property was measured, the two or more 10microC/cm value was acquired as a difference of reversal and a noninverting charge, and the good ferroelectric property was shown. The fatigue property, the maintenance property, etc. were good.
[0181] Moreover, when the property in the transistor of 0.26 micrometers of gate length was evaluated, p mold and n mold were 10% or less all over the wafer, and dispersion in a threshold Vt was good.

[0182] Furthermore, when resistance between the lower electrodes 13 and the 2nd metal wiring 10 which were connected through the capacity lower contact 12 of 0.4-micrometer angle was measured with the contact chain, the resistance per contact was 10ohms or less, and was good.
[0183] (Second operation gestalt) Next, the second operation gestalt of this invention is explained using drawing 9 and drawing 10 . Drawing 9 is the sectional view of the memory cell of the ferroelectric random-access memory concerning this operation gestalt, or DRAM, and drawing 10 is a sectional view of a part which a plate line connects with the 2nd metal wiring in the end.
[0184] Unlike the first operation gestalt, in this operation gestalt, the up electrode 15 of the ceramic thin film capacity 30 has an area smaller than the ceramic thin film 14 and the lower electrode 13. By making ceramic thin film capacity 30 into such structure, the defect that the up electrode 15 and the lower electrode 13 short-circuit in the capacity side-attachment-wall section can be prevented by poor etching of the ceramic thin film 14 and the lower electrode 13.
[0185] Moreover, the 3rd metal wiring 18 is connected with the 2nd metal wiring 10 through the lower electrode 13 and the capacity lower contact 12. By considering as such structure, the capacity up contact 17 and the plate line contact 19 serve as the almost same depth, and it becomes easy to form them in coincidence. Moreover, since a conductor of the same kind can be used for the target up electrode 15 and the target lower electrode 13 which connect the 3rd metal wiring 18, there is also an advantage of being easy to control the contact resistance to each.
[0186] Next, the manufacture approach of the memory concerning this operation gestalt is explained.
[0187] The process until it forms the up electrode 15 on the ceramic thin film 14 is completely the same as that of the case of the first operation gestalt. Then, the up electrode 15 is processed by etching. Under the present circumstances, an up electrode is removed by etching in the field of the plate line contact 19 shown in drawing 10 . Then, the 4th interlayer insulation film 16 is formed, and further, after puncturing the capacity up contact 17 and the plate line contact 19, the 3rd metal wiring 18 is formed.
[0188] (Third operation gestalt) Next, with reference to drawing 11 thru/or drawing 14 R> 4, the ferroelectric random-access memory or DRAM concerning the third operation gestalt of this invention is explained. Drawing 11 is the top view having shown the memory cell of the ferroelectric random-access memory concerning this operation gestalt, or DRAM. In addition, downward structure is the same as the structure shown in drawing 1 (A) than the 1st metal wiring. Drawing 12 is a sectional view in the B-B line of drawing 11 . Drawing 13 and drawing 1414 are sectional views of a part which connect a plate line with the 2nd metal wiring in the end.
[0189] Although the third operation gestalt is the same as the first operation gestalt about the point of having connected ceramic thin film capacity to a diffusion layer electrically according to the plug structure which connected metal wiring and beer, the structure and its manufacture approach of ceramic thin film capacity differ from the first operation gestalt.
[0190] The ceramic thin film capacity 30 in this operation gestalt consists the whole surface of the both sides of two or more lower electrodes 13 which opened spacing and were formed on the 3rd interlayer insulation film 11, and the 3rd interlayer insulation film 11 and the lower electrode 13 of a wrap ceramic thin film 14 and an up electrode 15 currently formed on the ceramic thin film 14 so that some lower electrodes [at least] 13 may be covered, as shown in drawing 12 . The up electrode 15 serves as the plate line 34 in drawing 3 .
[0191] Since it becomes unnecessary to form contact on the plate line 34 on the ceramic thin film capacity 30 by making ceramic thin film capacity 30 into such structure, the structure of ceramic thin film capacity is simplified and detailed-ization of a device can be performed easily.
[0192] Moreover, the effective area of the ceramic thin film capacity 30 can also be made to increase, without making the area of a cel increase by making the lower electrode 13 into three-dimensional configurations, such as a rectangular parallelepiped and telescopic.
[0193] Next, the manufacture approach of the memory concerning this operation gestalt is explained.
[0194] The manufacture approach about structures other than ceramic thin film capacity 30 is the same as the approach described in the first operation gestalt. For this reason, only the manufacture approach of the ceramic thin film capacity 30 is described below.

[0195] After forming the capacity lower contact 12, on the 3rd interlayer insulation film 11, membranes are formed by the sputtering method etc. and the lower electrode 13 is processed by etching. In order to obtain the good ceramic thin film 14, it is necessary to change the front face of the processed lower electrode 13 into the pure condition that there is no etching residue etc. Therefore, it is desirable to carry out washing processing of the front face of the lower electrode 13 with an organic solvent etc. after etching. On the lower electrode 13, the ceramic thin films 14, such as PZT and BST, are formed with a CVD method etc.

[0196] As shown in drawing 13 , in connecting the up electrode 15 which functions as a plate line 34 to the 2nd metal wiring 10, it punctures the plate line contact 19 after formation of the ceramic thin film 14.

[0197] In drawing 13 , although the plate line contact 19 runs through the ceramic thin film 14 and has arrived at the interior of the 3rd interlayer insulation film 11, the ceramic thin film 14 may be unable to be etched on the 3rd interlayer insulation film 11 and these conditions. In such a case, it is desirable to remove beforehand the ceramic thin film 14 of the periphery of the plate line contact 19 by etching.

[0198] Subsequently, after forming the up electrode 15 by the sputtering method etc., it is processed by etching and the ceramic thin film capacity 30 and the plate line 34 are formed. Besides, the passivation film (not shown) is formed.

[0199] As shown in drawing 14 , the up electrode 15 can also be connected to the 2nd metal wiring 10 through the lower electrode 13. In this case, after puncturing the plate line contact 19 after forming the ceramic thin film 14, and forming the up electrode 15 on it, it is processed by etching.

[0200] By two kinds of both approaches mentioned above, before forming the up electrode 15, it is necessary to etch the ceramic thin film 14. However, in the case of ferroelectric random-access memory, the interface of an electrode and the ferroelectric film influences the electrical characteristics of capacity greatly especially. Therefore, it is desirable, in order that not ashing but the approach of exfoliating with an organic solvent may not give a damage to the ceramic thin film 14 as an approach of exfoliating a resist after etching the ceramic thin film 14.

[0201] Moreover, it is desirable that the plate line contact 19 also punctures a resist by wet etching since it exfoliates easily.

[0202] It is also possible to connect the up electrode 15 to the 2nd metal wiring 10 through the 3rd metal wiring 18 like the first operation gestalt, without being based on such an approach.

[0203] In this operation gestalt, in order to form the ceramic thin film 14 after processing the lower electrode 13, the ceramic thin film 14 and the 3rd interlayer insulation film 11 under it react, or there is a possibility that the effect of the element which constitutes the ceramic thin film 14 being spread in the 3rd interlayer insulation film 11 etc. which is not desirable may come out. In such a case, it is desirable to prepare the diffusion barrier film (not shown) on the 3rd interlayer insulation film 11. Since the insulating metallic oxide of TaO2, TiO2, and ZrO2 grade of adhesion with the ceramic thin film 14 is good as diffusion barrier film, it is desirable.

[0204] Moreover, in this operation gestalt, in order to use the up electrode 15 as a plate line 34, there is a possibility that resistance of the plate line 34 may become high depending on the ingredient of the up electrode 15. Especially, since it is common in ferroelectric random-access memory to drive a plate line for writing and read-out of a memory cell, it is necessary to fully make the plate line 34 low resistance. In such a case, what is necessary is just to use the plate backing wiring 23 (for it not to appear in drawing 15 (B), since it is directly under the plate line 34), as shown in drawing 15 (B). Since the plate backing wiring 23 can be formed from the metal of low resistance, it can make resistance of the plate line 34 low enough.

[0205] Next, the concrete example at the time of applying this operation gestalt to ferroelectric random-access memory is explained using drawing 12 .

[0206] The manufacture process before formation of the ferroelectric capacity 30 is the same as that of the case of the example of the first operation gestalt.

[0207] On the 3rd interlayer insulation film 11, PZT capacity was manufactured by the following approaches.

[0208] First, TiN with a thickness of 50nm, Pt with a thickness of 50nm, and Ir with a thickness of 50nm were formed by sputtering in this order as a lower electrode 13. After applying a resist besides, pattern NINGU was carried out and the lower electrode 13 was etched by making Ar and Cl2 into reactant gas. Then, ashing removed the resist and washing processing was further carried out with the mixed solution of dimethyl sulfoxide and water.

[0209] Besides, the PZT thin film 14 with a thickness of 200nm was formed like the case of the example of the first operation gestalt. However, membrane formation time amount of PZT was made into 1200 seconds.

[0210] Subsequently, on the PZT thin film 14, spreading and after carrying out patterning, wet etching of the PZT film 14 was carried out for the resist with the FUTSU nitric acid, and the plate line contact 19 was formed.

[0211] Then, the resist was exfoliated with the organic solvent and annealing for 10 minutes was performed at the temperature of 400 degrees C under the ambient atmosphere of 100% of oxygen.

[0212] Subsequently, IrO2 of 50nm of thickness and Ir of 100nm of thickness were formed by the sputtering method as an up electrode 15 on the PZT film 14 at this order.

[0213] Then, annealing for 10 minutes was performed at the temperature of 400 degrees C under the ambient atmosphere of 100% of oxygen, and it considered as the PZT capacity 30.

[0214] Silicon oxide was formed by O3 TEOS-CVD as the 4th interlayer insulation film 16. After forming the SiON film by plasma CVD as passivation film (not shown) besides, the polyimide film was formed further. Finally, the wiring pad section was punctured.

[0215] Ferroelectric random-access memory equipped with the cel array which accumulated about 16,000 memory cells shown in drawing 3 by the above-mentioned approach, a sense amplifier, a decoder, etc. was manufactured. This ferroelectric random-access memory checked operating in supply voltage 2.5V and 100 or less ns of cycle times.

[0216] (Fourth operation gestalt) Next, the ferroelectric random-access memory or DRAM concerning the fourth operation gestalt of this invention is explained with reference to drawing 15 and drawing 16 . Drawing 15 (A) is the top view of a memory cell, until after forming the 2nd metal wiring, and drawing 15 (B) is the top view which omitted the device formed before the 1st metal wiring 7 of those other than diffusion layer 4. Drawing 16 is a sectional view in the C-C line of drawing 15 (A).

[0217] With this operation gestalt, the structure of metal wiring in the plug which connects the ceramic thin film capacity 30 to a diffusion layer 4, and beer differs from the first operation gestalt. That is, with this operation gestalt, although the capacity lower contact 12 is formed in right above [of beer 9] with the first operation gestalt, as shown in drawing 16 , in the die-length direction of the 2nd metal wiring 10, beer 9 and the capacity lower contact 12 open fixed spacing, and are arranged. That is, the capacity lower contact 12 is not formed in right above [of beer 9].

[0218] Depending on the formation process of beer 9 and the 2nd metal wiring 10, a crater etc. may be generated in the 2nd metal wiring 10 on beer 9. Thus, when the capacity lower contact 12 and 2nd beer 20 grade are formed on the 2nd metal wiring 10 which the crater produced and which is not flat, there is a possibility that good electrical installation may not be obtained. For this reason, in such a case, it is desirable like this operation gestalt to form capacity lower contact 12 grade in the location which separated only fixed spacing from beer 9 instead of right above [of beer 9].

[0219] Moreover, as shown in drawing 16 , the capacity lower contact 12 is not located in the center of the ceramic thin film capacity 30. Moreover, the capacity up contact 17 which has connected the ceramic thin film capacity 30 and the 3rd metal wiring 18 is not arranged right above [of the capacity lower contact 12]. Even if a crater etc. is generated on the capacity lower contact 12 by arranging the capacity lower contact 12 and the capacity up contact 17 in this way, it does not have a bad influence on the property of the ceramic thin film capacity 30. Furthermore, it does not have a bad influence on the electrical installation between the 3rd metal wiring 18 and the up electrode 15, either. Moreover, cel area is not made to increase.

[0220] The memory concerning this operation gestalt can be manufactured by the same approach as the memory concerning the first operation gestalt.

[0221] (Fifth operation gestalt) Next, the ferroelectric random-access memory or DRAM concerning the fifth operation gestalt of this invention is explained with reference to drawing 17 and drawing 18 . Drawing 17 is the top view having shown the memory cell of the ferroelectric random-access memory concerning this operation gestalt, or DRAM, and shows downward structure from the 2nd contact 21. Upper structure is the same as the structure shown in drawing 1 (B) than the 2nd contact 21. Drawing 18 is a sectional view in D-D line of drawing 1717 .

[0222] In this operation gestalt, the 2nd metal wiring 10 and a diffusion layer 4 are directly connected through the 2nd contact 21 in the plug which connects the ceramic thin film capacity 30 and a diffusion layer 4, without connecting the ceramic thin film capacity 30 and the 1st metal wiring 7.

[0223] Since the 1st metal wiring 7 is used for both the capacity plug which connects the ceramic thin film capacity 30 and a diffusion layer 4, and the bit line, it needs to be separated from the capacity plug and the bit line of the 1st metal wiring 7 at spacing processible by etching with the first operation gestalt. On the other hand, since the 1st metal wiring 7 is used only as a bit line 35 into the cel with this operation gestalt, it is possible for the capacity plug and the bit line not to be separated at the above spacing, therefore to make cel area reduce.

[0224] Next, the manufacture approach of the memory concerning this operation gestalt is explained.

[0225] First, even the 1st metal wiring 7 and the 2nd interlayer insulation film 8 are formed like the first operation gestalt. However, the contact for connecting capacity is not formed. Next, the 2nd contact 21 is punctured by etching. Then, although barrier metal, such as Ti and TiN, is formed, since especially an aspect ratio becomes large, it is desirable [the 2nd contact 21] to embed like collimator sputtering or a CVD method and to form membranes by the good method of forming sexual.

[0226] Next, a tungsten plug is formed like the case where contact 6 is formed. The beer in the 2nd contact 21 and other multilayer metal wiring can also be formed in coincidence. Thus, the 2nd metal wiring 10 is formed after the 2nd formed contact 21. Subsequent processes are the same as the first operation gestalt.

[0227] (Sixth operation gestalt) The ferroelectric random-access memory or DRAM which starts the sixth operation gestalt of this invention next is explained with reference to drawing 19 .

[0228] Although the memory cell of not connecting the ceramic thin film capacity 30 and the 1st metal wiring 7 concerning this operation gestalt is the same as that of the fifth operation gestalt in the plug which connects the ceramic thin film capacity 30 and a diffusion layer 4, as shown in drawing 19 , the 2nd metal wiring 10 is connected to a diffusion layer 4 through beer 9 and contact 6.

[0229] Also in this operation gestalt, like the fifth operation gestalt, since the 1st metal wiring 7 is used only as a bit line 35 into the cel, it is possible to make cel area reduce. And since the 2nd contact 21 is not used unlike the fifth operation gestalt, a manufacture process can be simplified.

[0230] Next, the manufacture approach of the memory concerning this operation gestalt is explained.

[0231] Even the 1st interlayer insulation film 5 is formed like the first operation gestalt. Next, although the 1st metal wiring 7 is formed, the 1st metal wiring 7 of a capacity plug is not formed (that is, as shown in drawing 19 , the 1st metal wiring 7 is not formed on a diffusion layer 4).

[0232] Subsequently, beer 9 is punctured by etching after forming the 2nd interlayer insulation film 8 after the 1st interlayer insulation film 5 and the 1st metal wiring 7.

[0233] In multilayer metal wiring of those other than a memory cell, although even the 1st metal wiring 7 is etched, by the memory cell, over etching of the 2nd interlayer insulation film 8 is carried out even to the 1st interlayer insulation film 5.

[0234] Next, a tungsten plug is formed like the case where contact 6 is formed. Thus, the 2nd metal wiring 10 is formed on the formed beer 9. Subsequent processes are the same as the first operation gestalt.

[0235] (Seventh operation gestalt) Next, the ferroelectric random-access memory or DRAM concerning the seventh operation gestalt of this invention is explained with reference to drawing 20 thru/or drawing 23 . Drawing 20 is the top view having shown the memory cell of the ferroelectric random-access memory in this operation gestalt, or DRAM, and shows downward structure rather than the 1st metal wiring. Drawing 21 is a sectional view in the E-E line of drawing 20 .

[0236] With this operation gestalt, the silicide wiring 22 is used as a bit line 35, and the 1st metal wiring 7 is used only in the plug which connects the ceramic thin film capacity 30 and a diffusion layer 4. For this reason, it is possible like the fifth operation gestalt to make cel area reduce.
[0237] Moreover, with this operation gestalt, the 1st metal wiring 7 and the 2nd metal wiring 10 are used as backing wiring of a word line 33.
[0238] Drawing 22 is the circuit diagram showing connection of backing wiring and a word line 33, and drawing 23 is the top view of the connection of the 1st metal wiring 7 and a word line 33.
[0239] Since a word line 33 mainly consists of polish recon, its resistance is high. Therefore, generally backing metal wiring of low resistance to a word line 33, and lowering resistance of a word line 33 to it is performed. Such backing wiring usually uses metal wiring of one layer. On the other hand, the word line 33 is backed in this operation gestalt, without making cel area increase by using two-layer metal wiring as backing wiring.
[0240] Furthermore, as shown in drawing 22 , the array connected with a word line 33 is divided two, and the noise is reduced by considering as symmetrical structure by the array which divided metal wiring which backs.
[0241] Next, the manufacture approach of the memory concerning this operation gestalt is explained.
[0242] First, the transistor section is formed on a silicon substrate 1 like the case of the first operation gestalt. After forming an interlayer insulation film (not shown), contact 6 is punctured and the silicide wiring 22 is formed by WSi etc. The 1st interlayer insulation film 5 is formed on this interlayer insulation film, and the 2nd contact 21 is punctured on a diffusion layer 4 after that. Subsequent processes are the same as the first operation gestalt.
[0243]
[Effect of the Invention] As explained above, according to this invention, ceramic thin film capacity is connected with a diffusion layer through the plug which consists of structure which carried out the laminating of formation of multilayer metal wiring, the beer formed in coincidence, and the metal wiring. For this reason, based on such a basic configuration, the semiconductor device using the ceramic thin film capacity which can form multilayer metal wiring easily and does not produce degradation of a capacitative element, either can be offered.
[0244] The reason is that formation of multilayer metal wiring is not barred for the difference of elevation by this ceramic thin film capacity in order to form ceramic thin film capacity after multilayer metal wiring formation.
[0245] Furthermore, since there is no need for formation of contact between metal wiring and a substrate and formation of the beer by the tungsten plug after ceramic thin film capacity formation, there is no degradation of ceramic thin film capacity.
[0246] Moreover, after forming multilayer metal wiring, and before forming ceramic thin film capacity, a deterioration of the transistor can be reduced by performing hydrogen annealing.
[0247] Moreover, according to this invention, the semiconductor device which loaded together the memory using ceramic thin film capacity and a large-scale logical circuit on the same chip by low cost is offered. It is because ceramic thin film capacity can be formed, without changing the process device of the logical circuit section in any way, so the existing design parameter can be used.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing 1 (A) and (B) are the top views showing the memory cell concerning the 1st operation gestalt of this invention.
[Drawing 2] It is the sectional view which met the A-A line of drawing 1 (A).
[Drawing 3] It is the circuit diagram of the memory concerning the 1st operation gestalt shown in drawing 1 .
[Drawing 4] It is the sectional view showing the manufacture approach of the memory concerning the 1st operation gestalt of this invention.
[Drawing 5] It is the sectional view showing the manufacture approach of the memory concerning the 1st operation gestalt of this invention.
[Drawing 6] It is the sectional view showing the manufacture approach of the memory concerning the 1st operation gestalt of this invention.
[Drawing 7] It is the sectional view showing an example of the structure of the end of the plate line in the memory concerning the 1st operation gestalt of this invention.
[Drawing 8] It is the sectional view showing other examples of the structure of the end of the plate line in the memory concerning the 1st operation gestalt of this invention.
[Drawing 9] It is the sectional view of the memory concerning the 2nd operation gestalt of this invention.
[Drawing 10] It is the sectional view showing an example of the structure of the end of the plate line in the memory concerning the 2nd operation gestalt of this invention.
[Drawing 11] It is the top view showing the memory concerning the 3rd operation gestalt of this invention.
[Drawing 12] It is a sectional view in the B-B line of drawing 11 .
[Drawing 13] It is the sectional view showing an example of the structure of the end of the plate line in the memory concerning the 3rd operation gestalt of this invention.
[Drawing 14] It is the sectional view showing other examples of the structure of the end of the plate line in the memory concerning the 3rd operation gestalt of this invention.
[Drawing 15] Drawing 15 (A) and (B) are the top views showing the memory concerning the 4th operation gestalt of this invention.
[Drawing 16] It is a sectional view in the C-C line of drawing 15 (A).
[Drawing 17] It is the top view showing the memory concerning the 5th operation gestalt of this invention.
[Drawing 18] It is a sectional view in D-D line of drawing 17 .
[Drawing 19] It is the sectional view showing the memory concerning the 6th operation gestalt of this invention.
[Drawing 20] It is the top view showing the memory concerning the 7th operation gestalt of this invention.
[Drawing 21] It is a sectional view in the E-E line of drawing 20 .

[Drawing 22] It is the circuit block diagram of the memory concerning the 7th operation gestalt of this invention.
[Drawing 23] It is the top view showing the connection of the word line of the memory concerning the 7th operation gestalt of this invention, and the 1st metal wiring which is word line backing wiring.
[Description of Notations]
1 Silicon Substrate
2 Silicon Oxide
3 Gate
4 Diffusion Layer
5 1st Interlayer Insulation Film
6 Contact
7 1st Metal Wiring
8 2nd Interlayer Insulation Film
9 Beer
10 2nd Metal Wiring
11 3rd Interlayer Insulation Film
12 Capacity Lower Contact
13 Lower Electrode
14 Ceramic Thin Film
15 Up Electrode
16 4th Interlayer Insulation Film
17 Capacity Up Contact
18 3rd Metal Wiring
19 Plate Line Contact
20 2nd Beer
21 2nd Contact
22 Silicide Wiring
30 Ceramic Thin Film Capacity
31 Selection Transistor
32 Memory Cell
33 Word Line
34 Plate Line
35 Bit Line

[Translation done.]

* NOTICES *

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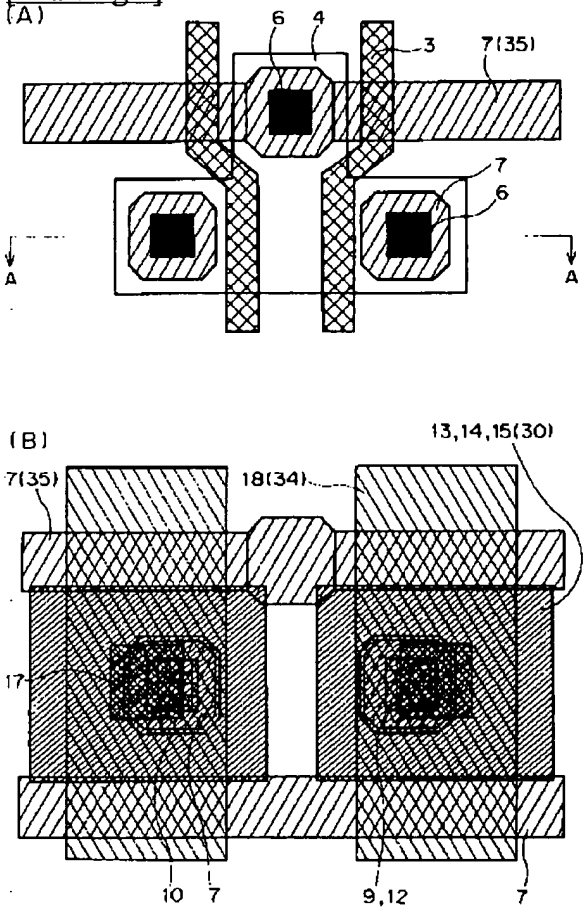
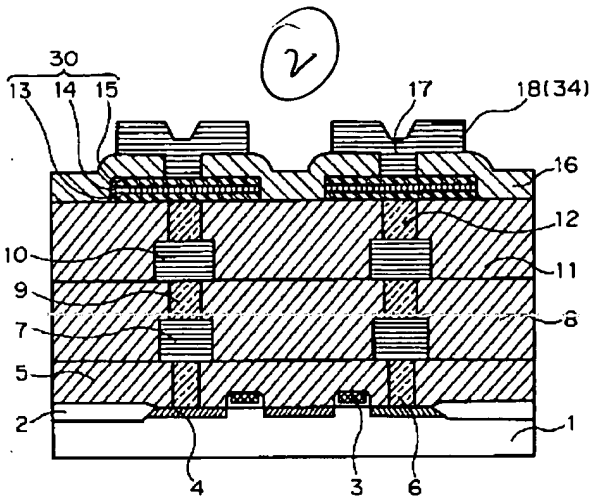
3.In the drawings, any words are not translated.

DRAWINGS

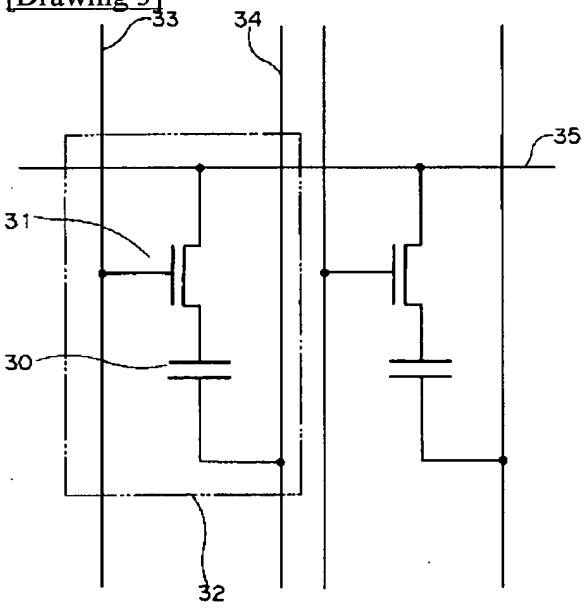
[Drawing 1]



[Drawing 2]



[Drawing 3]



[Drawing 5]

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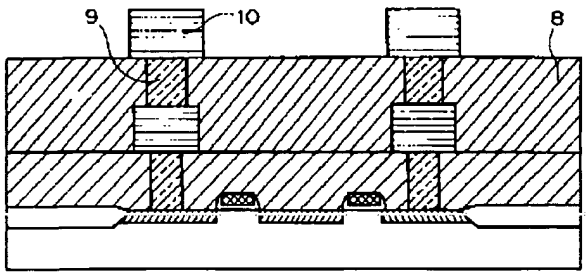

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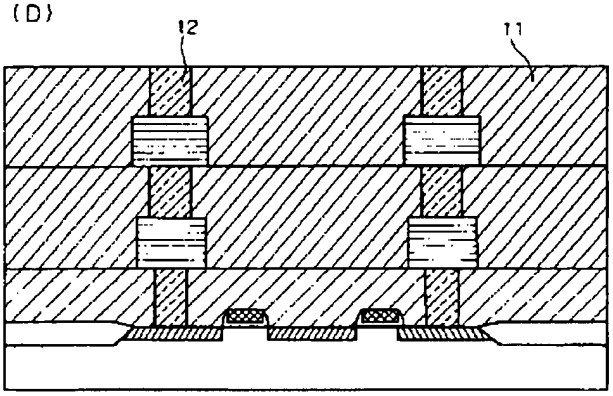

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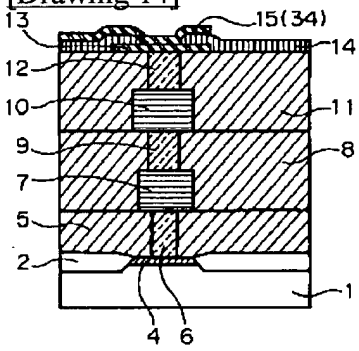

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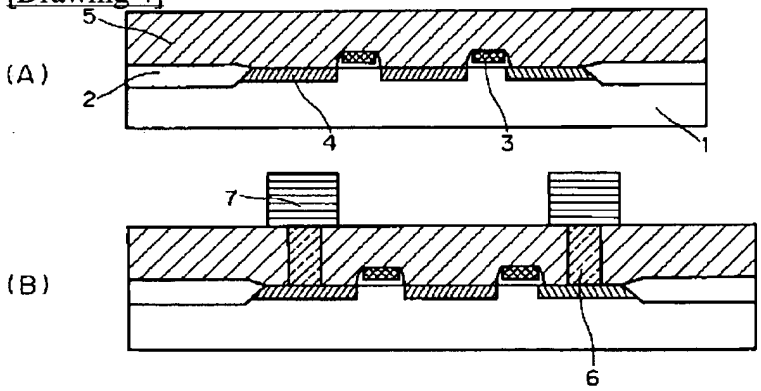

[Drawing 6]

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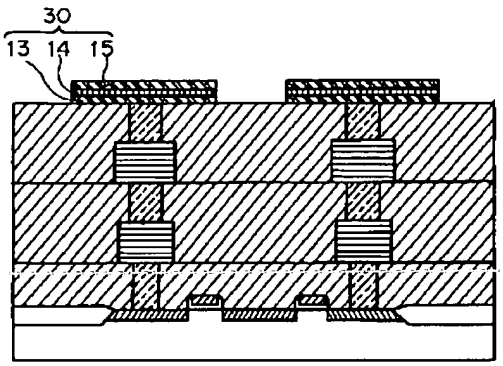

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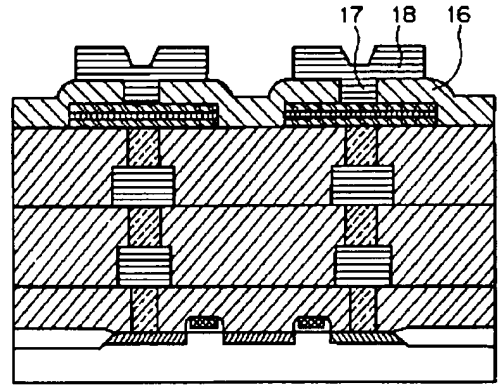

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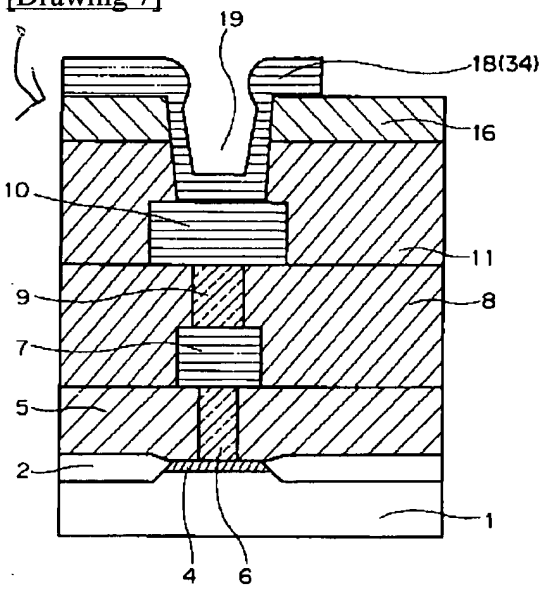

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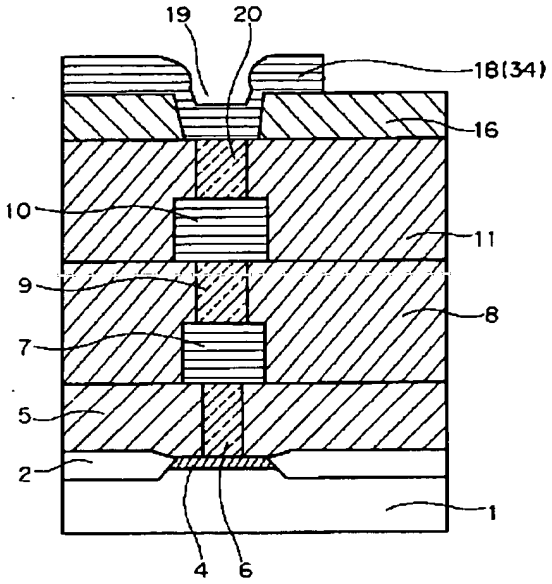

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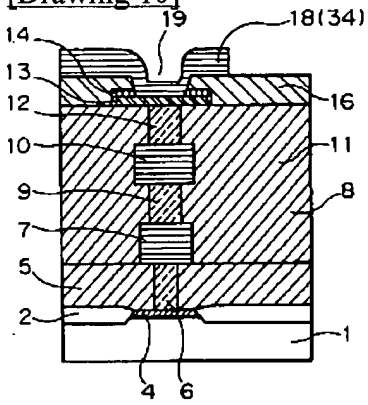

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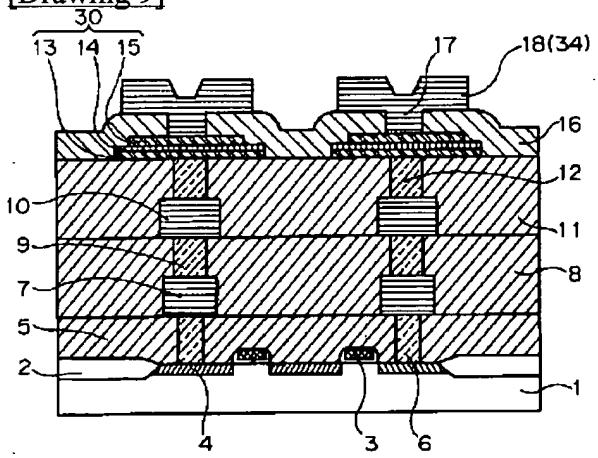

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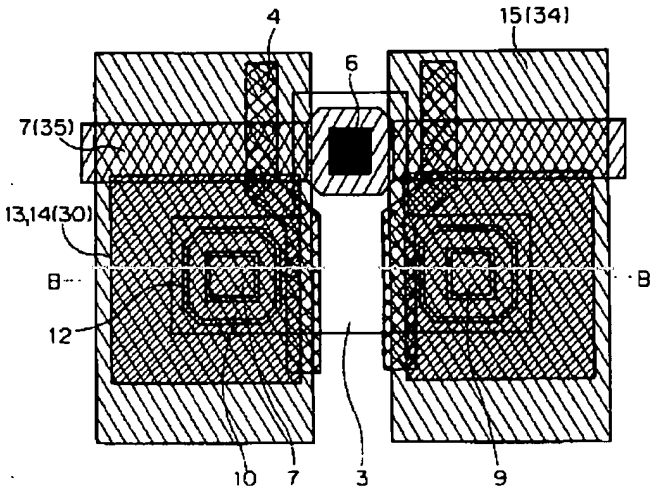

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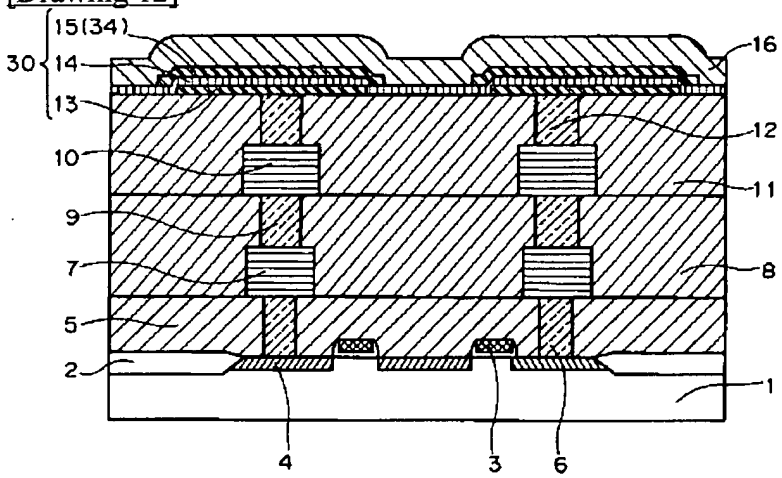

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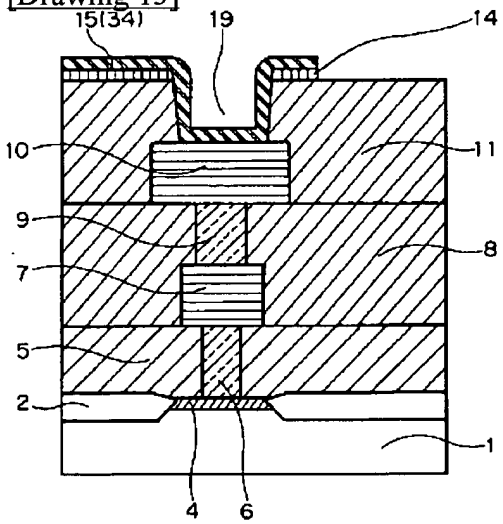
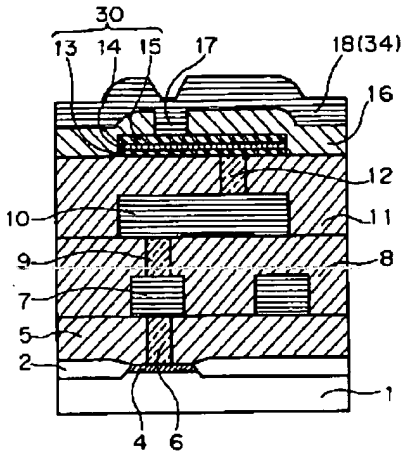
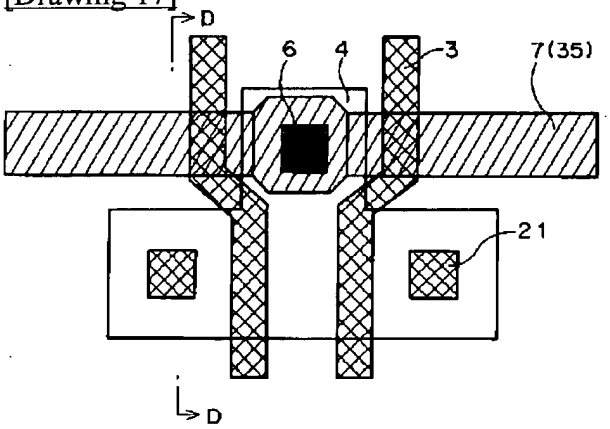


[Drawing 16]

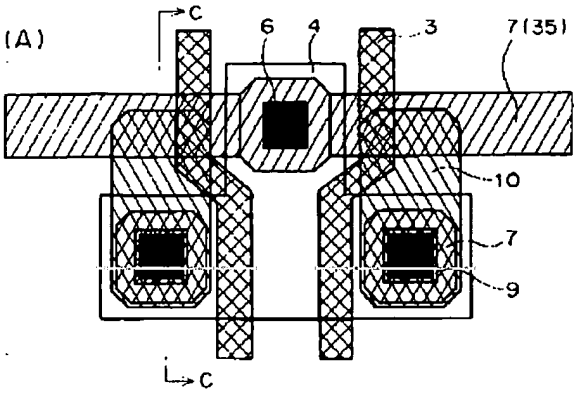


[Drawing 17]



[Drawing 15]

(A)



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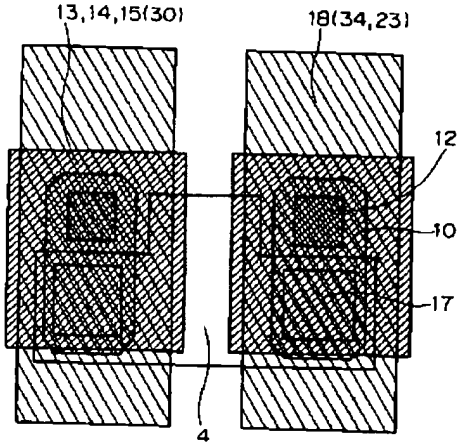

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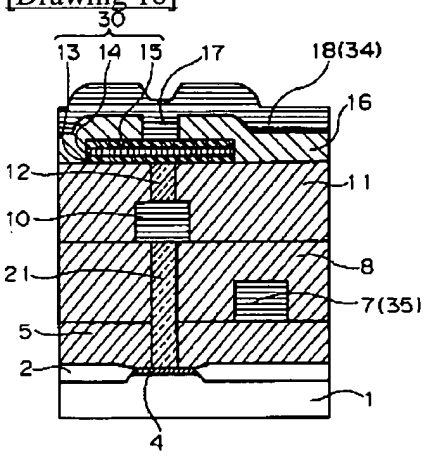

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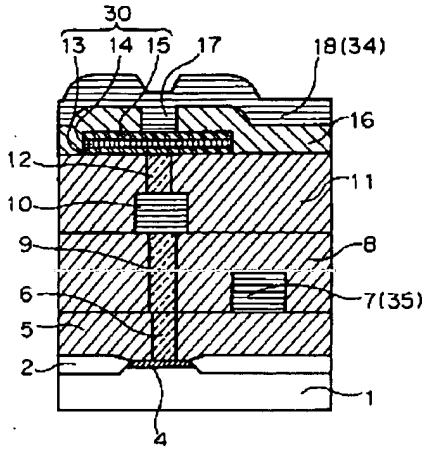

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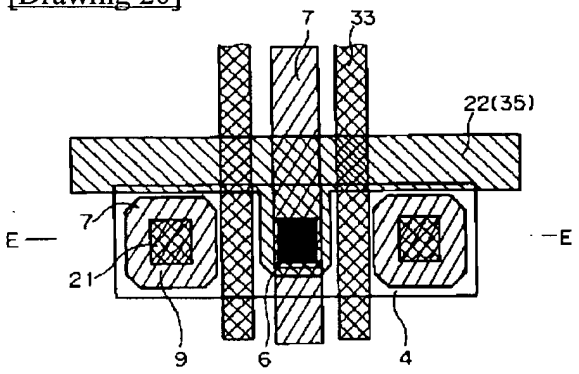
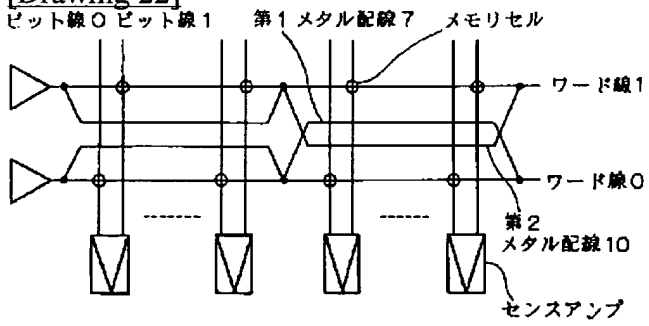
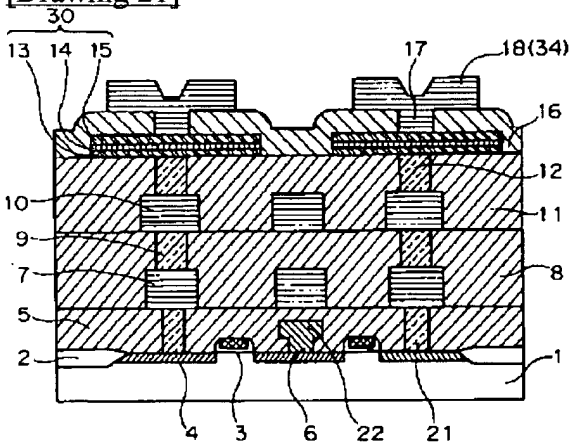


[Drawing 22]



[Drawing 21]



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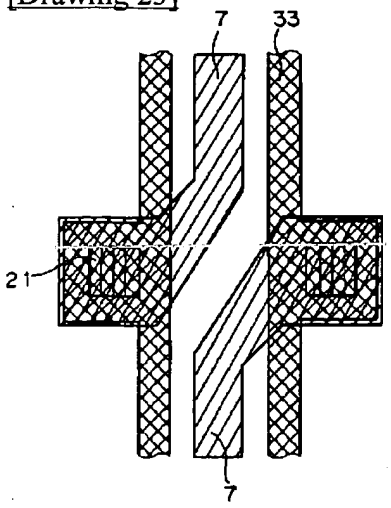

[Translation done.]